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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/615,298

07/09/2003

Osamu Furukawa

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09/21/2005

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EXAMINER

CARPIO, IVAN HERNAN

ART UNIT

PAPER NUMBER

2841

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/615,298

Applicant(s)

FURUKAWA ET AL.

Examiner

Ivan H. Carpio

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>7-9-03</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2 are rejected under 35 U.S.C. 102(e) as being unpatentable over Huang (US Patent 6777819).

With respect to claim 1 Huang teaches a surface-mounted electronic component module (Fig. 1) comprising: a wiring substrate (Fig.1, element 20) having wiring patterns (Fig.1, elements 202) formed on one side and external connection terminals (Fig. 1, elements 203) formed on the other side, the wiring patterns and the external connection terminals being connected with each other by via holes (paragraph [0016], lines 6-8) or through holes; a plurality of electronic component devices (Fig. 1, element 21 and 22) mounted on the one side of the wiring substrate; and an exterior resin layer (Fig. 1, element 26) formed on the wiring substrate which covers the plurality of electronic component devices, wherein at least one of the plurality of electronic component devices (Fig.1, element 21) is fastened face up to the one side of the wiring

substrate, the connection terminal of the electronic component device fastened face up and the wiring pattern or the connection terminal of another electronic component device being connected with each other by wire (Fig.1, element 23).

With respect to claim 2 and with all the limitations of claim 1, Huang teaches that at least one of the wire bondings connecting the connection terminal of the electronic component device fastened face up and the wiring pattern or the connection terminal of the another electronic component device, has a predetermined inductance (Fig. 1, element 23 Note that any circuit element including wire can have a predetermined inductance) as a circuit element.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Fujimoto (US Patent 6777819).

With respect to claim 3 and with all the limitations of claim 1, Huang teaches that an electronic component device fastened face up to the one side of the wiring substrate but does not specify that it is attached by a conductive paste. Fujimoto teaches a component device attached face up to a substrate by a conductive paste (paragraph

[0039], lines 1-4). It would have been obvious to attach the electronic component to the substrate taught by Huang using the conductive paste taught by Fujimoto for the purpose of conducting heat away from the component.

With respect to claim 4 and with all the limitations of claim 2, Huang teaches that an electronic component device fastened face up to the one side of the wiring substrate but does not specify that it is attached by a conductive paste. Fujimoto teaches a component device attached face up to a substrate by a conductive paste (paragraph [0039], lines 1-4). It would have been obvious to attach the electronic component to the substrate taught by Huang using the conductive paste taught by Fujimoto for the purpose of conducting heat away from the component.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US Patent 6784765) in view of Huang.

With respect to claim 5, Yamada teaches a surface mounted electronic component module (Fig. 4) comprising, a wiring substrate (Fig. 4, elements 19, 15 and 16) having wiring patterns (Fig. 4, elements 2) formed on one side and external connection terminals (Fig. 4, elements 7) formed on the other side, the wiring patterns and connection terminals being connected to each other with via holes (Fig. 4, elements 3), a semiconductor chip (Fig. 4, element 4) mounted on the one side of the wiring substrate and forming a switch (column 12, lines 15-20) for changing over the opening/closing of radio frequency transmission/reception signals and a decoder circuit (fig. 4, elements 2) for controlling the switch changeover operations; a surface acoustic

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wave filter (Fig. 4, element 5) connected to the switch, an exterior resin layer (Fig. 4, element 6) formed on the wiring substrate which covers the semiconductor chip and the surface acoustic wave filter. Yamada does not teach wherein at least one of the semiconductor chip and the surface acoustic wave filter is fastened face up to the one side of the wiring substrate, the connection terminal of the at least one of the semiconductor chip and the surface acoustic wave filter, fastened face up, and the wiring pattern or the connection terminal of the other being connected with each other through wire bonding. Huang teaches a semiconductor device (Fig.1, element 21) that is mounted face up the one side of the wiring substrate and that the connection terminal of the semiconductor chip is connected to the wiring pattern by wire bonding (Fig. 1, element 23). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the mounting structure taught by Huang on the RF device taught by Yamada because doing so would make the positioning of the chips on the wiring substrate more flexible since wires of any length can be used.

With respect to claim 6 and with all the limitations of claim 5, Yamada teaches that the connection terminals connected through the wire bonding are signal terminals (Fig.1, the connection terminals can always be signal terminals), the wire bonding having a predetermined inductance (Fig.1, note that any electrical element can have a predetermined inductance including a wire) as a circuit element.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada and Huang in view of Fujimoto (US Patent 6777819).

With respect to claim 7 and with all the limitations of claim 5, Yamada and Huang teach all of the limitations except that at least one of the semiconductor chip and the surface acoustic wave filter, fastened to the one side of the wiring substrate, is fastened to the wiring substrate by a bond made of conductive paste. Fujimoto teaches a component device attached face up to a substrate by a conductive paste (paragraph [0039], lines 1-4). It would have been obvious to attach the electronic component to the substrate taught by Yamada using the conductive paste taught by Fujimoto for the purpose of conducting heat away from the component.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 6713375 discloses an RF device for use in a cellular phone, US Patent 6794747 discloses a semiconductor device on a ceramic substrate.

Conclusion

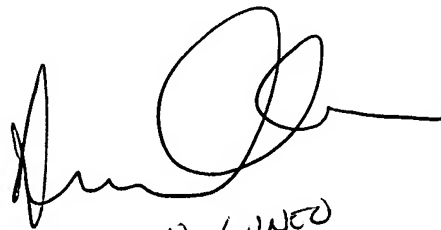
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ivan H. Carpio whose telephone number is 571-272-8396. The examiner can normally be reached on M-R 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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